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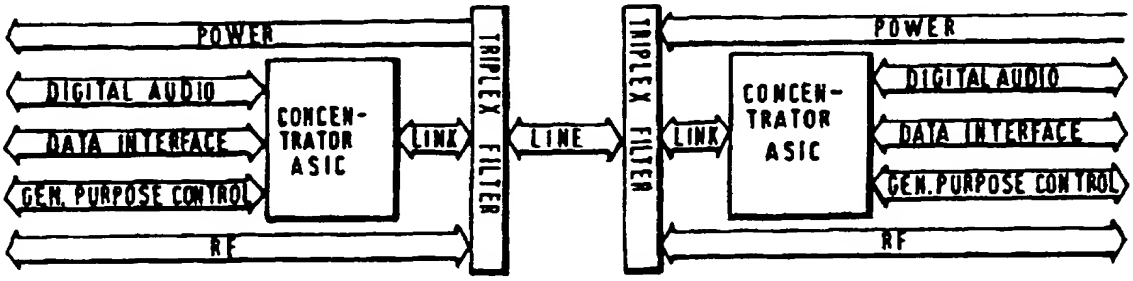

(57) Abstract

A cellular telephone including a signal concentrator system for connection of an associated accessory by means of a two-wire link, whereby a plurality of different types of signals may be transmitted over the same link, the concentrator comprising means for converting the signals of different types to a single type of signal, means for transmitting the combined signal over the said link, and means for receiving the combined signal and extracting the signals of different types from it.

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SIGNAL CONCENTRATOR FOR CONNECTION BETWEEN CELLULAR TELEPHONE AND ASSOCIATED ACCESSORIES

This invention relates to a connection system for use between the handset of a cellular telephone, and accessories such as a data modem.

A terminal connection for use with a telephone system, for example to allow data to be transmitted over the PSTN, may be required to deal with three main types of digital signals:

(1) "DAI" (Digital Audio Interface) outputs for serial transmission;

(2) "V24" (standard computer communications) serial interface; and

(3) "I/O Port Interface" (e.g. for system control signals).

Such links commonly require a multi-way connection, for example, containing as many as 25 wires in the case of a fully implemented RS232-V24 connector.

Accordingly, the present invention provides a concentrator system for linking a cellular telephone and an accessory that enables a plurality of signal connections of different kinds to be provided over the same two wire link. Preferably these include external power, digital audio, digital I/O and external antenna connections.

A preferred embodiment of the present invention provides a concentrator system comprising a pair of

concentrators each providing a plurality of interfaces for different categories of signals to be transmitted and received between them over the same two wire link, with one acting as a master and the other acting as a slave. Preferably the master concentrator is adapted to be incorporated in the handset of a cellular telephone.

Preferably, the interfaces comprise a DAI (Digital Audio Interface), a UART (asynchronous communication) interface, and an I/O port interface.

Preferably, the output from each concentrator is also combined with power and RF lines by means of a triplex filter.

Preferably, the UART interface in the master concentrator is arranged to handle two logical channels of communication, comprising (a) the end-to-end serial communication over the link, and (b) control communications between a CPU in the handset, and the master concentrator itself.

In addition, the I/O port interface is preferably arranged to be accessible as an internal register over the UART control channel.

Preferably, the DAI interface is adapted to allow connection of a peripheral audio interface to the handset, with A/D and D/A conversion being achieved by means of an externally situated CODEC.

Preferably, the UART interface provides the following functions:

(1) Connection of terminal equipment to a remote modem over GSM data service using a circuit or packet oriented connection;

(2) Connection of external equipment to the mobile handset such as a voice-dialer;

(3) Connection of terminal equipment with SMS/CBS capabilities;

(4) Testing and programming of the mobile handset; and

(5) Communication between the microcontroller's core processor and the internal registers of the master concentrator.

Preferably, the I/O interface provides eight input and eight output general purpose ports. These are adapted to allow connection of various external control signals, for example to detect "ignition sense" in a car system, or to provide a warning signal via the car's horn when there is an incoming call to the handset.

As mentioned above, two logical communication channels must be mapped over the physical link, to allow access to the concentrator registers over the UART boundary, by the microcontroller, in parallel with serial data exchange between a terminal and the mobile handset. In order to avoid delaying or slowing down data exchange, and also to avoid the requirement for modem control signals to be used for handshaking between the concentrator and the microcontroller (on which modem control signals may not be available) the control frames and data frames are preferably

interleaved. Thus the bit rate of the UART on the master side is preferably twice the bit rate on the slave side, to ensure that the end-to-end bit rate is equal to the slave side rate.

However, because the data flow on a DTE to DCE serial interface is typically a series of bursts, rather than a steady flow, the scheme is preferably not such that alternate frames are always a control frame and a data frame, which could lead to an infinite access time between control accesses to the master concentrator. Instead the preferred transmission scheme allows possible sequences of (a) control frame - data frame or (b) control frame - control frame, the first bit of the control frame being arranged to indicate whether the next frame is a control frame or a data frame.

Preferably, the different interfaces which are served by the concentrator, share the link between the master and the slave concentrators by means of a time division multiplexing scheme and communication is performed in a half duplex mode, so that the master and slave concentrators cannot drive the link simultaneously.

Preferably, the data frames are allotted to the different interfaces, on a "round robin" basis, but alternatively, each frame may be arranged to transmit a "dribble" of bits from each of the low bit rate interfaces, and in any case, the DAI is preferably allotted at least part of each data frame, whenever it is active.

Some embodiments of the invention will now be described by way of example, with reference to the accompanying drawings in which:

Figure 1 illustrates a first type of framing scheme for link communication;

Figure 2 illustrates an exchange of set-up frames between concentrators;

Figure 3 illustrates an alternative frame structure;

Figure 4 illustrates a "test mode" frame format;

Figure 5 illustrates a protocol for entering the test mode;

Figure 6 illustrates a sequence of synchronisation frames;

Figure 7 illustrates the architecture of a concentrator ASIC;

Figure 8 illustrates the architecture of the UART interface;

Figure 9 is a diagram showing UART receive timing;

Figure 10 is a diagram showing UART transmit timing;

Figure 11 illustrates the architecture of the UART communication controller;

Figure 12 illustrates the scheme of communication between the micro controller and the master concentrator;

Figure 13 illustrates the architecture of an analog device compatible DAI;

Figure 14 shows timing diagrams for the DAI of Figure 13;

Figure 15 illustrates the architecture of the link controller;

Figure 16 is an overall schematic diagram of a conventional cellular handset system connector; and

Figure 17 is an overall schematic diagram of a connector according to the present invention.

Referring firstly to Figures 16 and 17 which illustrate the basic difference between a conventional connector and that of the invention, it will be seen from Figure 16 that a number of connection lines are required in the conventional arrangement, to connect between the mobile telephone and any external equipment, via a multi-way system interface. In the concentrator arrangement of the present invention, Figure 17, the Digital Audio Interface, Data Interface, and general purpose control signals are concentrated together and then applied together with power and RF connections, to a triplex filter which connects to the 2-wire link.

Figure 1 illustrates a possible framing scheme for link communication. This illustrates a "round robin" allocation of frame space, to the lower rate interfaces, while the digital signal processor interface is allocated 13 bits from each frame. Thus, for example, a frame is sent from the master to the slave containing 10 bits of UART data and 13 bits of DAI data, followed by a frame returning from the slave to the master with the same allocation of bits. The next frame transmitted from the master to the slave

contains 8 bits of I/O port data followed by 13 bits of DAI data, and again, the following frame from the slave to the master, contains the same allocation of bits.

Figure 2 illustrates the exchange of frames when the master concentrator configures the slave concentrator with a set-up frame. The slave connector replies with a set-up frame simply to maintain the mechanism of sending and receiving the same types of frames.

Figure 3 illustrates an alternative frame format, in which, once again, each frame contains a 13 bit sample from the DAI, but instead of the "round robin" scheme for allocating the other bits, these contain a dribble of bits from each of the low bit interfaces in every frame. For example, the C and U fields contain data from the UART interface, while the M and I bits carry 1 bit each of data from the modem control lines and from the I/O port interface.

Figure 4 illustrates the test mode frame format, in which only data from the UART interface is transmitted. As can be seen from Figure 5, a special protocol is employed for entering the test mode, in which a set up test mode frame is sent from the master to the slave first, followed by a set up reply frame from the slave to the master, after which the sequence of test mode frames is followed by a "break frame" from the master to the slave, followed by a test mode from the slave to the master, which terminates the sequence.

Figure 6 illustrates the arrangement for achieving frame synchronisation between the master and slave concentrators, and the arrangement is such that after a reset, the connection is always initiated by the master in response to a demand for a connection from the controlling CPU in the mobile handset. After receiving a complete sync frame, the slave concentrator responds with a sync frame of its own. As illustrated in the drawing, the master will continue to transmit sync frames, until it receives a proper response from the slave.

Since the line used for link communication between the mobile handset and external equipment is a multi-mode line, carrying antenna signals, power supply and link data, the encoding of the link data bits must not contain any DC component, and signalling must be two level. Accordingly, pseudo ternary codes are not suitable, and the preferred system uses the diphase or Manchester code, as used on a normal 10 megabit per second ethernet network.

Figure 7 illustrates the overall architecture of an ASIC embodying the concentrator which is basically the same for both master and slave. Each concentrator is configured dynamically on power-up to be either a master or a slave and the figure corresponds to that of the master concentrator, in which UART communication controller 2 handles the UART command protocol used between the master concentrator and the microcontroller processor, via a register bank 4 on which the UART communication controller can perform read and

write operations. Thus the slave concentrator arrangement will differ, in that the connection through the UART communication controller from the UART to the link, is short-circuited.

In operation, when a framing signal is received on the DAI of the master concentrator, the link controller is forced to load a frame into the serial transmit register and to transmit the frame to the slave concentrator. The slave concentrator receives this frame and responds to the master with a frame including a DAI sample, together with modem control signals, data from the UART, data from the I/O ports, or set-up data.

The UART communication controller acts in response to events generated by the UART interface, or by the link controller, i.e. the arrival of new data from either side. The UART communication controller in the master concentrator keeps track of the type of frames to be sent and received on the UART interface, and in this way commands transmitted from the microcontroller over the UART interface can be filtered out of the stream of UART data presented to the link controller. The stream of UART data from the link is interleaved with command frames.

In the slave concentrator, the UART communication controller is inactive, and simply relays UART data from link to UART and vice versa. The UART interface reacts asynchronously to valid start pits on the RX line, or to incoming data for transmission to the transmit buffer. The

DAI interface acts synchronously on receiving the frame signal and starts exchange of DAI samples with the DAI processor.

Figure 10 illustrates the architecture of the UART interface itself. The UART architecture is composed of three main elements: registers, counters and a controller. The bit rate is generated by a programmable clock divider which generates a clock of 16 times the bit rate. From this clock the receive and transmit timing is generated in 2 modulo 16 counters. This enables the receive clock and transmit clock to be enabled disabled asynchronously.

Reception of data is performed as follows. The length of the receive shift register is initially set up to the chosen data format. The length is controlled by Parity, 7/8 bit and 1/2 stop bit signals. These signals simply control multiplexers that can bypass flip-flops in the shift register and thereby adjust the length. The length of the receive shift register is the same as the length of the chosen data format including stop bits. The default value in the receive shift register is all bits equal to logical one. The input line is continuously sampled with 16 times the bit rate. When a start bit level is detected on the line, the start bit signal is asserted by the start bit block and in response the controller enables the modulo 16 counter by asserting the enable receive signal. The character is then shifted in to the receive shift register. When the start bit reaches the end of the register the RSR

full signal is asserted. This causes the controller to negate the enable receive signal, which disables and resets the counter, and to assert the load RB signal for one MCLK cycle enabling the transfer of the received character to the receive buffer.

When the data is transferred to the receiver buffer the RSR full signal is negated. The receive timing is illustrated in Figure 9. Transmission of data is performed as follows. When the UART communication controller loads new data for transmission in the transmit buffer, the TBF signal is asserted. The data loaded in the transmit buffer is padded with stop bits if the chosen data is shorter than the longest format (8 bits + 1 parity bit). After receiving the TBF signal the controller asserts the load TSR signal for one MCLK cycle and asserts enable transmit. The load TSR signal clears the TBF signal. The bit-clock generator and the bit counter are enabled until the bit-counter has counted the number of bits transmitted in the chosen data format excluding stop bits. Then the frame sent is asserted causing the controller to negate enable transmit, which disables bit-clocking and resets the counters. The transmit timing is illustrated in Figure 10.

The UART interface has to be able to send and detect BREAK signals. The BREAK signal is basically a framing error of the received or transmitted character. In other words a start bit is received or transmitted instead of a stop bit at the end of the character frame. Therefore a

BREAK signal can be detected by examining the received stop bit/bits depending on the data format. In the UART architecture of Figure 10 the BREAK signal is sampled by the control when the RSR full signal is asserted. If the BREAK signal at this time is asserted the Break Out signal is asserted. This signal is conveyed to the opposite concentrator via the link controller and a modem control slot frame. The transmission of a break signal is done by forcing the output of the transmit shift register to start bit level during the next character transmitted after the break signal is received and keeping the output at this level for at least two stop bit periods.

In Figure 11 the architecture for the UART communication controller is depicted. The operation of the UART communication controller is as follows. Initially the first data received and transmitted through the UART is command frames. When the UART Rx buffer full flag RBF is set the communication controller sets the in multiplexer to a C1 frame and asserts the local bus buf and clear RBF signals for one MCLK cycle. This causes the expected command frame to be loaded into the leftmost part of the ADD./Data register and the clearance of the RBF flag. Depending on the CD bit and the type of frame (C1 or NOP) the next frame that arrives will either be loaded into left part of the Add./Data register (C1 frame or NOP), into the right part of the Add./Data register (C2 frame) or into the Link UART Tx. register (UART data frame). If the command

received is a write operation, then the command will be written to the addressed register when the C2 frame has been loaded. If the frame received is a read command then the addressed register is loaded in to the Com.Out register. A multiplexer controls whether the frame sent to the microcontroller is a NOP frame, a C1 frame or a C2 frame. Figure 12 shows the timing for receiving the C1 and C2 frames that together compose a write command for the simple case where no data frames are pending.

Figure 13 shows the architecture for an analog device compatible DAI. It will be appreciated that this is only one example of possible architecture. On the master concentrator the VSDOFS signal is generated by the baseband converter. On the slave the signal is generated by the concentrator. This is how the 8 KHz sampling signal is synchronised at both ends of the link. The interface is compatible with the ADSP 2100 family DAI's serial interfaces in thirteen bit mode with normal framing. VSCLK is always an input to the concentrator CVSDO can be tristated (not shown in figure 13). The interface works as follows. When VSDOFS goes high data on both CVSDO and CVSDI are clocked on the next high transition on VSCLK. Therefore the incoming data is latched on the low transitions. On the slave concentrator VSDOFS is generated when the link writes data to the transmit buffer and thereby asserting TBF. On the next high transition on VSCLK TBF is clocked on to the VSDOFS signal. This causes the controller to load the

serial transmit register. This clears the TBF flag. Thus on the next high transition on VSCLK VSDOFS is negated. The timing of the DAI interface is shown in Figure 14.

Figure 15 shows the architecture of the link. The link is the transceiver that receives and transmits data on the physical link and handles framing/deframing of data and communication with the various interfaces on the concentrator. The main components of the link are: serial transmit and receive registers in which packets are assembled/disassembled and shifted to and from the line decoder or encoder; line encoder, decoder that handles the Manchester encoding or decoding of bits; modulo 25/10 counter that detects the end of frames; selectors that control what data is received/transmitted in the packet; register buffers to different interfaces; a controller that is composed of state machines and finally a test mode frame rate generator and some additional logic. The serial registers are basically parallel to serial converters. The transmit serial register is clocked by the Manchester encoder which generates the link bit rate from a clock of twice the bit rate. The serial receiver register is clocked by the Manchester decoder which extracts the bit timing from the received packet. End of frame is detected by the bit counter. This signals to the controller to switch to reception when transmitting a frame and to load the receive registers and switch to transmission when receiving. The controller in the master concentrator synchronises

transmission with the reception of new data in the DAI transmit register in normal mode and with the internal generated frame rate when in test mode. The controller in the slave concentrator synchronises with the reception of frames from the master.

CLAIMS

1. A cellular telephone including a signal concentrator system for connection of an associated accessory by means of a two-wire link, whereby a plurality of different types of signals may be transmitted over the same link, the concentrator comprising means for converting the signals of different types to a single type of signal, means for transmitting the combined signal over the said link, and means for receiving the combined signal and extracting the signals of different types from it.

2. A cellular telephone according to claim 1 in which the converting and extracting means each comprise a plurality of signal interfaces including a digital audio interface ("DAI"), an asynchronous connection interface (UART) and an I/O port interface.

3. A cellular telephone according to claim 2 in which the combined signal is transmitted over the link in an asynchronous mode.

4. A cellular telephone system in accordance with claim 3 comprising a pair of concentrator devices one of which is arranged to act as a master and the other as a slave, the master being arranged in the handset of the cellular telephone.

5. A cellular telephone in accordance with claim 4 in which the UART interface in the master concentrator is arranged to handle two logical channels of information, which comprise (a) the end-to-end serial communications over the link and (b) communications between a CPU in the handset, and the master concentrator itself.

6. A cellular telephone according to claim 2 in which the I/O port interface is arranged to be accessible as an internal register over the UART control channel.

7. A cellular telephone according to claim 2 in which the I/O interface comprises a plurality of general purpose input and output ports.

8. A cellular telephone according to claim 4 in which the DAI interface is adapted to allow connection of a peripheral audio interface to the handset, and an external CODEC is provided to achieve A/D and D/A conversion.

9. A cellular telephone according to claim 3 in which the data is transmitted as discrete data frames interleaved with control frames.

10. A cellular telephone according to claim 9 in which the transmission scheme is arranged to allow sequences of frames in which some data frames may be omitted, whereby a

series of successive control frames may be transmitted between bursts of data when the data flow is intermittent.

11. A cellular telephone in accordance with claim 9 in which the different interfaces share the link between the master and slave concentrators by means of a time division multiplexing scheme and communication is performed in a half duplex mode so that the master and slave concentrators cannot drive the link simultaneously.

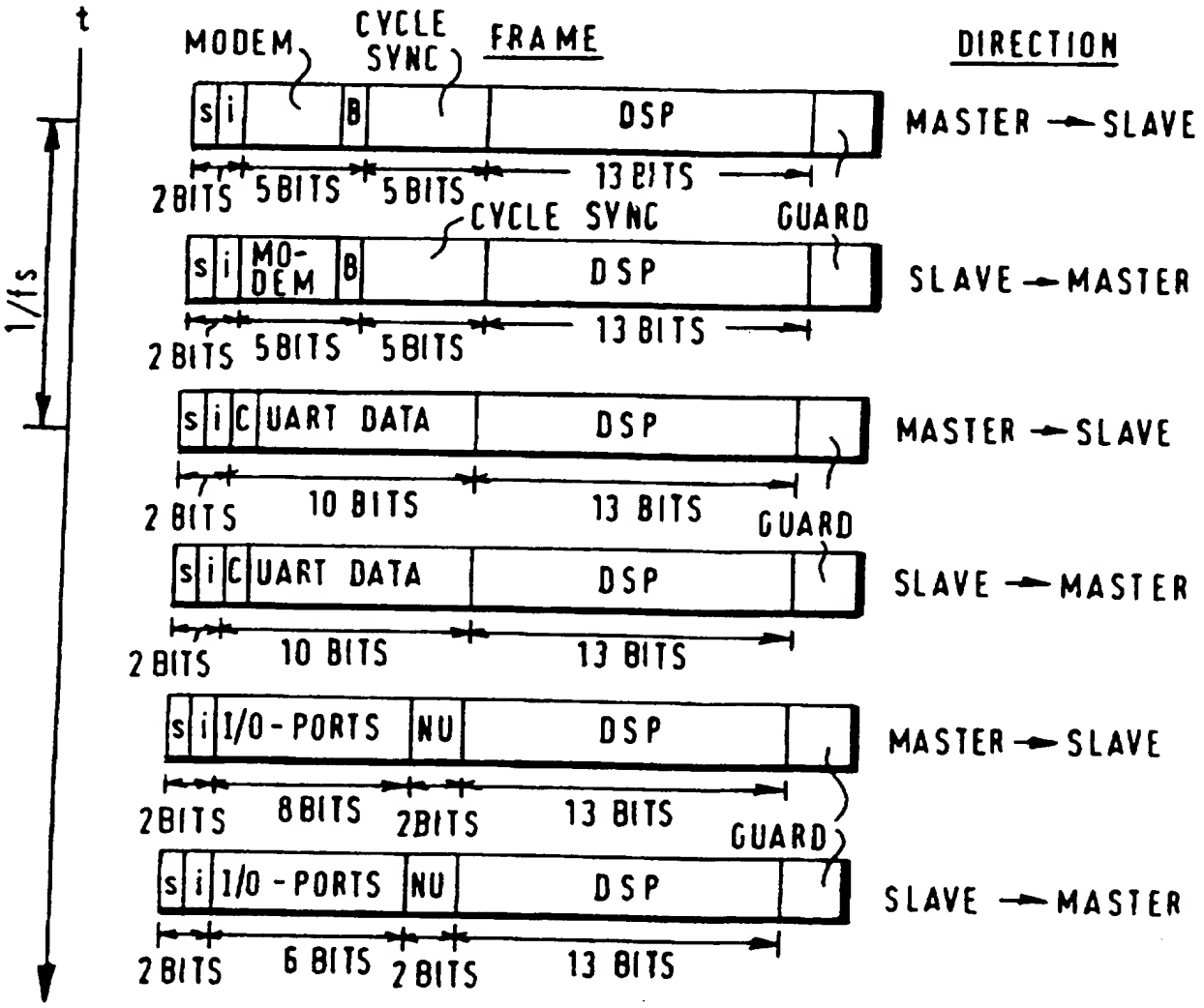
12. A cellular telephone according to claim 9 in which data frames are allotted to the different interfaces on a "round robin" basis.

13. A cellular telephone according to claim 9 in which the DAI interface is allotted at least part of each data frame when it is active, while the remainder of the frame comprises data from the other interfaces, allocated on a "round robin" basis.

14. A cellular telephone according to claim 9 in which the DAI interface is allotted at least part of each data frame when it is active, while the remainder of the frame comprises a dribble of bits from each of the low bit rate interface.

15. A cellular telephone system in accordance with any preceding claim in which the output from the concentrator is also combined with power and RF lines by means of a triplex filter.

FIG.1


t
1/fs
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MASTER → SLAVE
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SLAVE → MASTER
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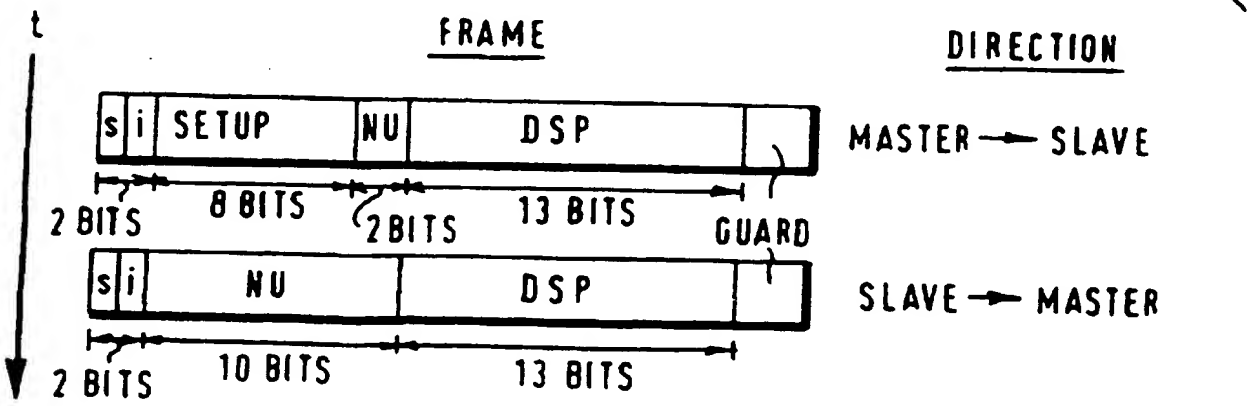
s i C UART DATA
DSP
MASTER → SLAVE
2 BITS 10 BITS 13 BITS
GUARD
s i C UART DATA
DSP
SLAVE → MASTER
2 BITS 10 BITS 13 BITS
s i I/O - PORTS NU
DSP
MASTER → SLAVE
2 BITS 8 BITS 2 BITS 13 BITS
GUARD
s i I/O - PORTS NU
DSP
SLAVE → MASTER
2 BITS 6 BITS 2 BITS 13 BITS

FIG. 2


t
FRAME
DIRECTION
s i SETUP NU
DSP
MASTER → SLAVE
2 BITS 8 BITS 2 BITS 13 BITS
GUARD
s i NU
DSP
SLAVE → MASTER
2 BITS 10 BITS 13 BITS

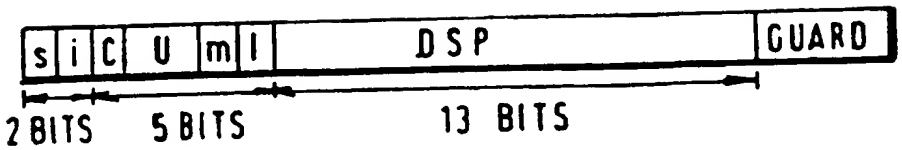


FIG.3

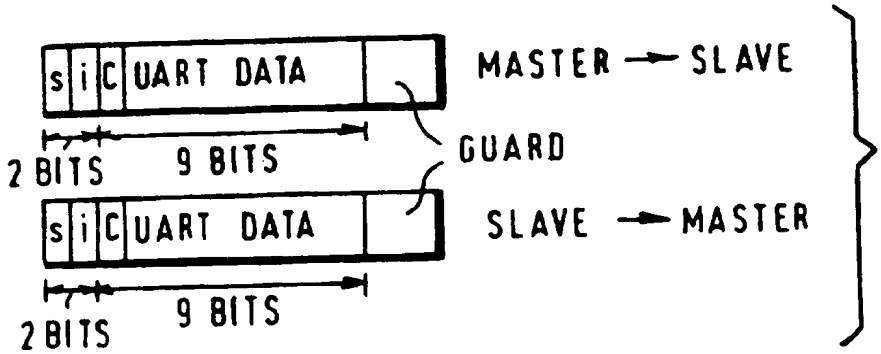


FIG.4

FIG.5

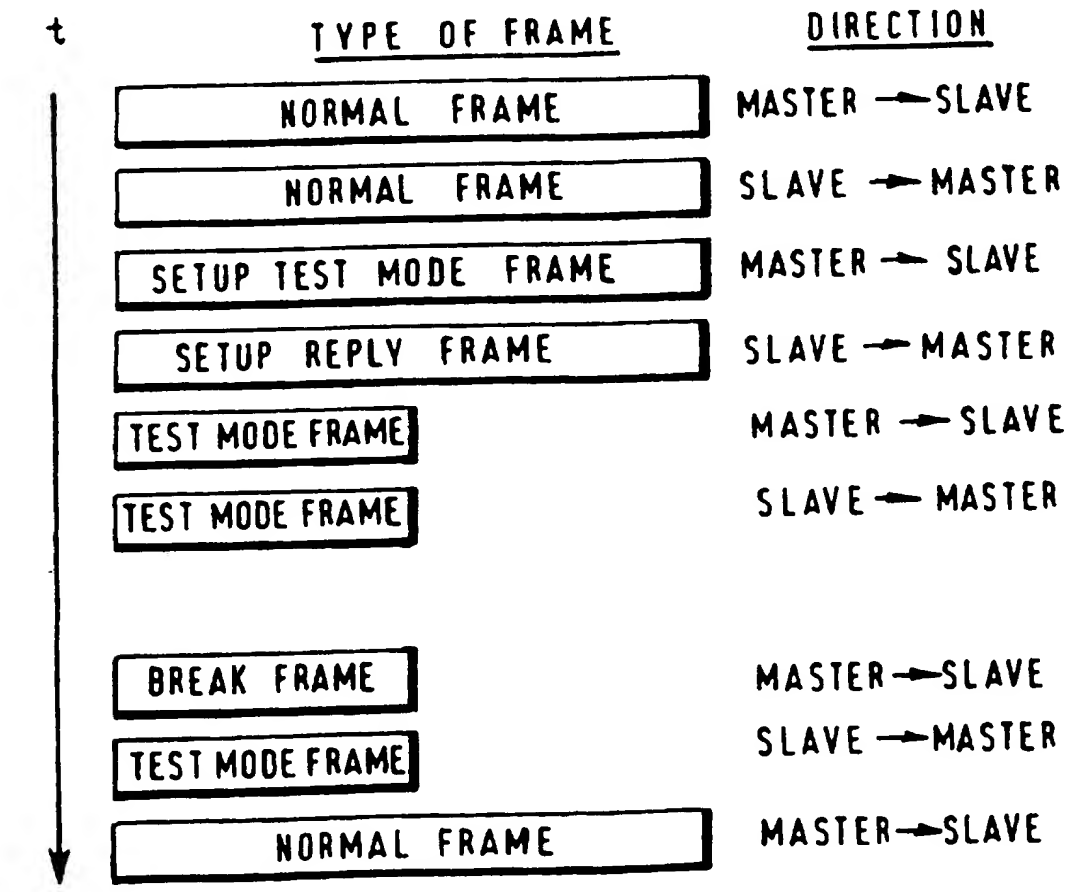


FIG. 6

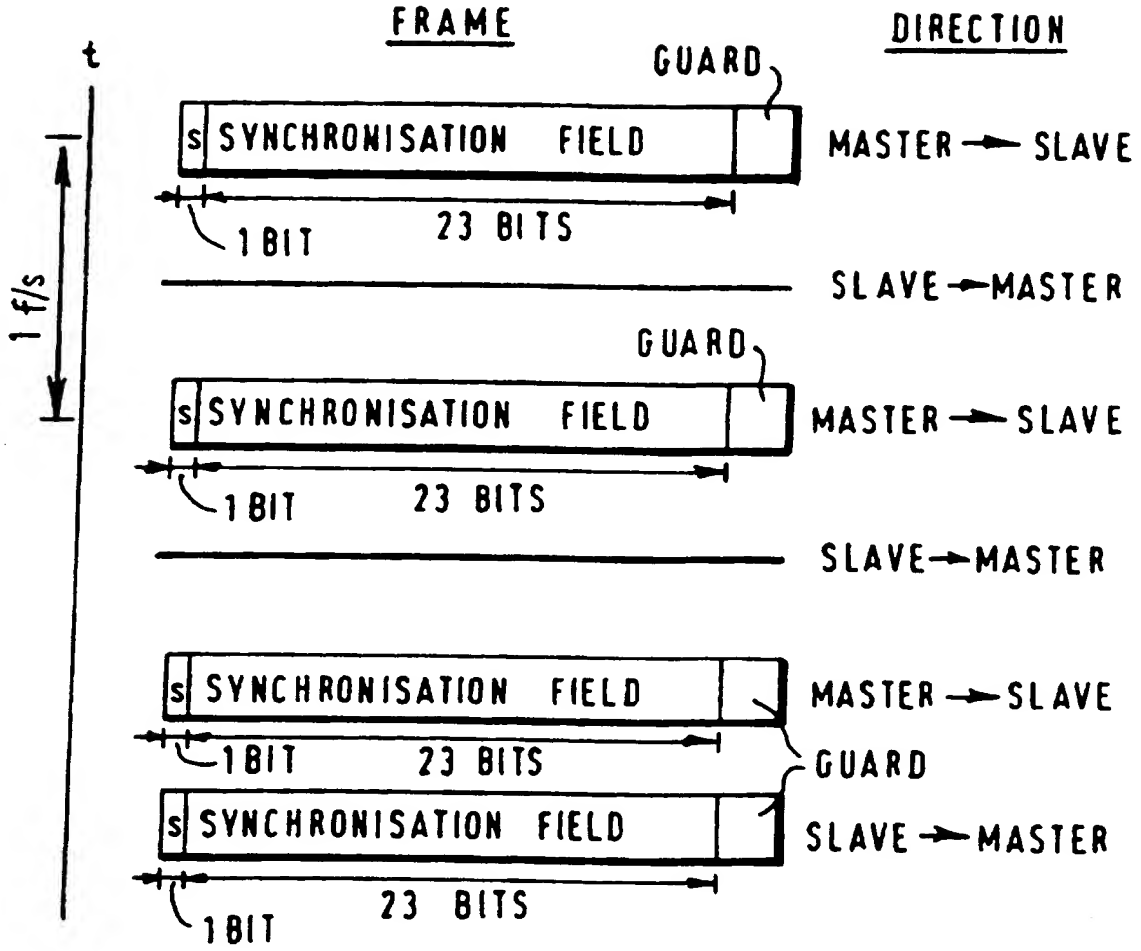
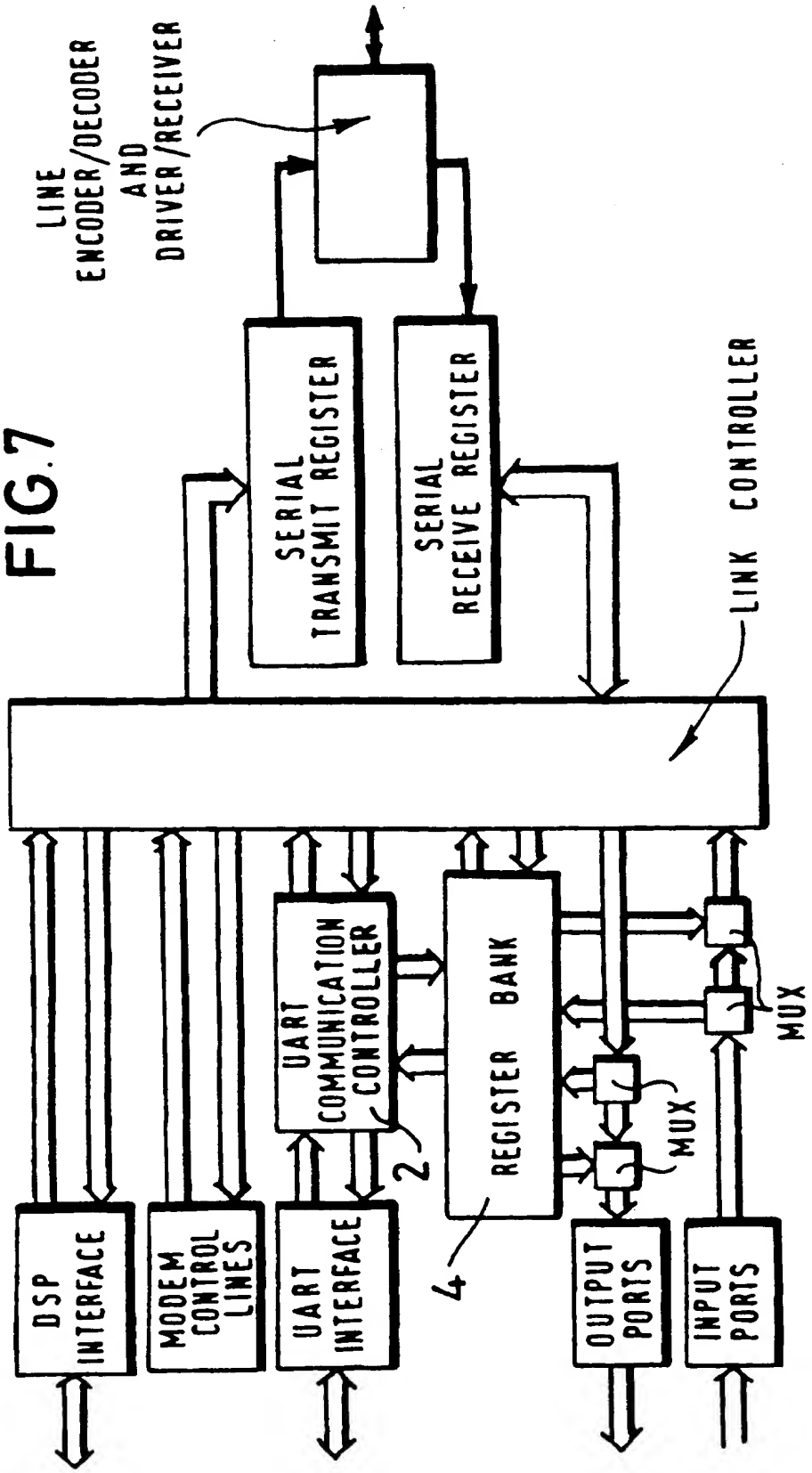


FIG.7


LINE ENCODER/DECODER AND DRIVER/RECEIVER
SERIAL TRANSMIT REGISTER
SERIAL RECEIVE REGISTER
LINK CONTROLLER
UART COMMUNICATION CONTROLLER
REGISTER BANK
MUX
MUX
DSP INTERFACE
MODEM CONTROL LINES
UART INTERFACE
OUTPUT PORTS
INPUT PORTS
2
4

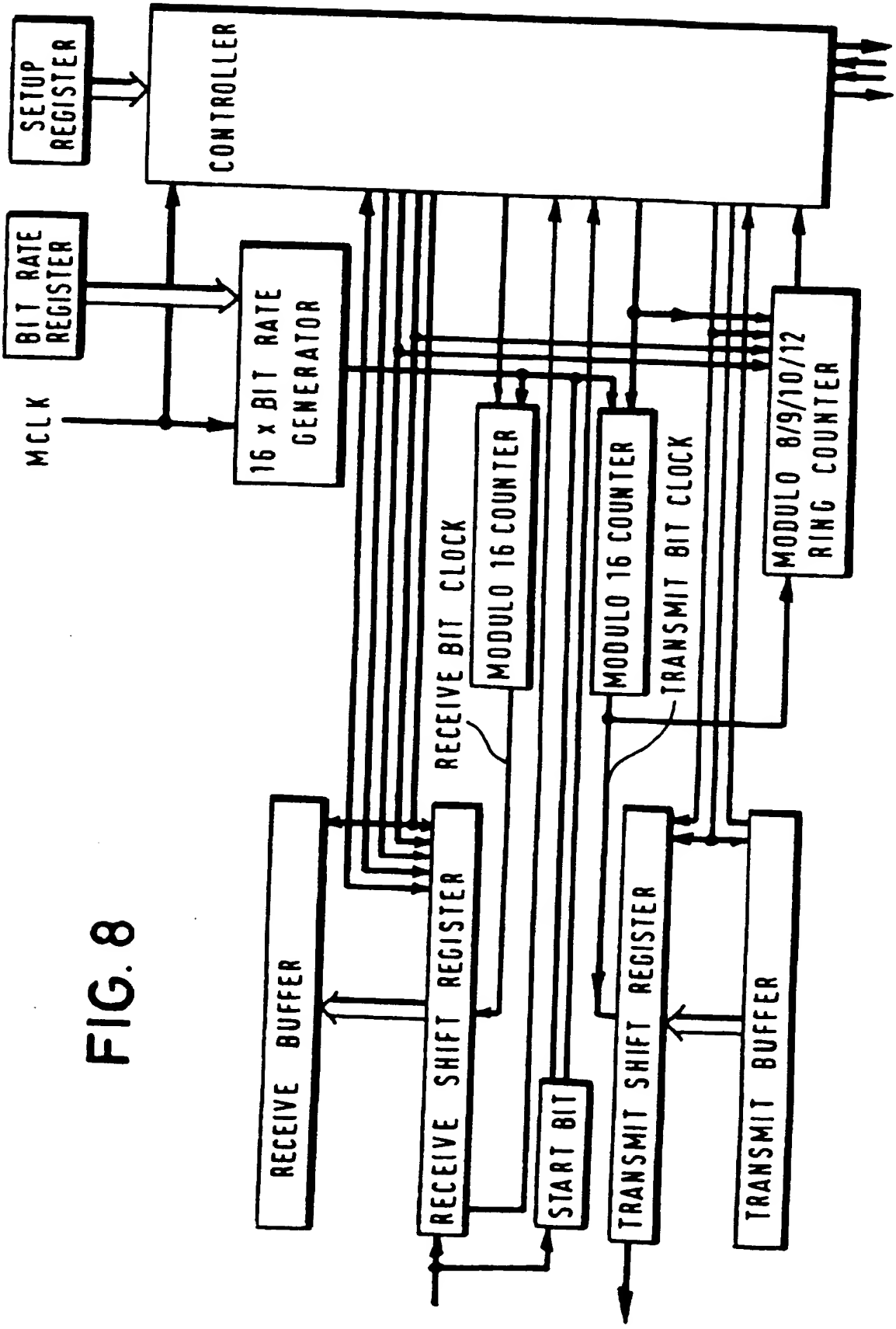


FIG. 8

FIG.9

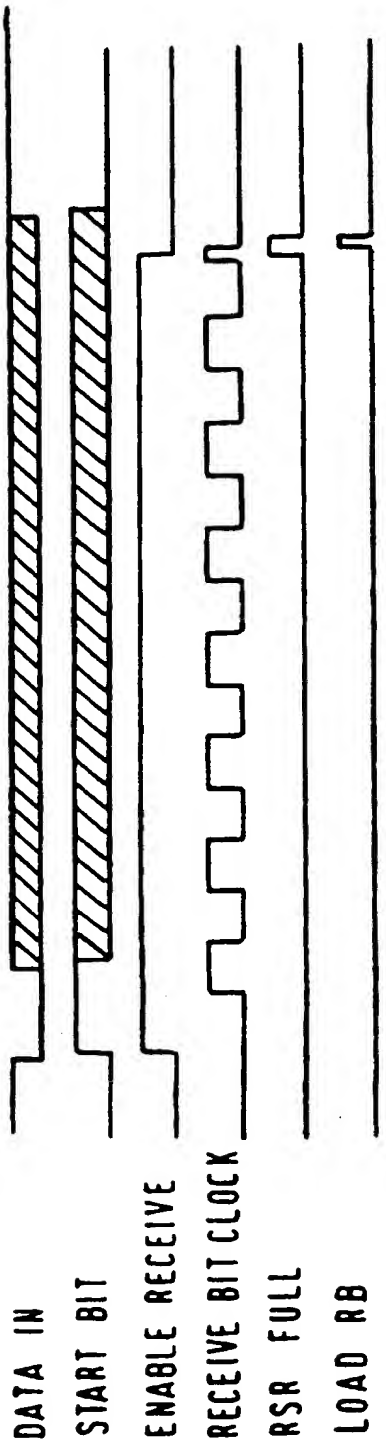
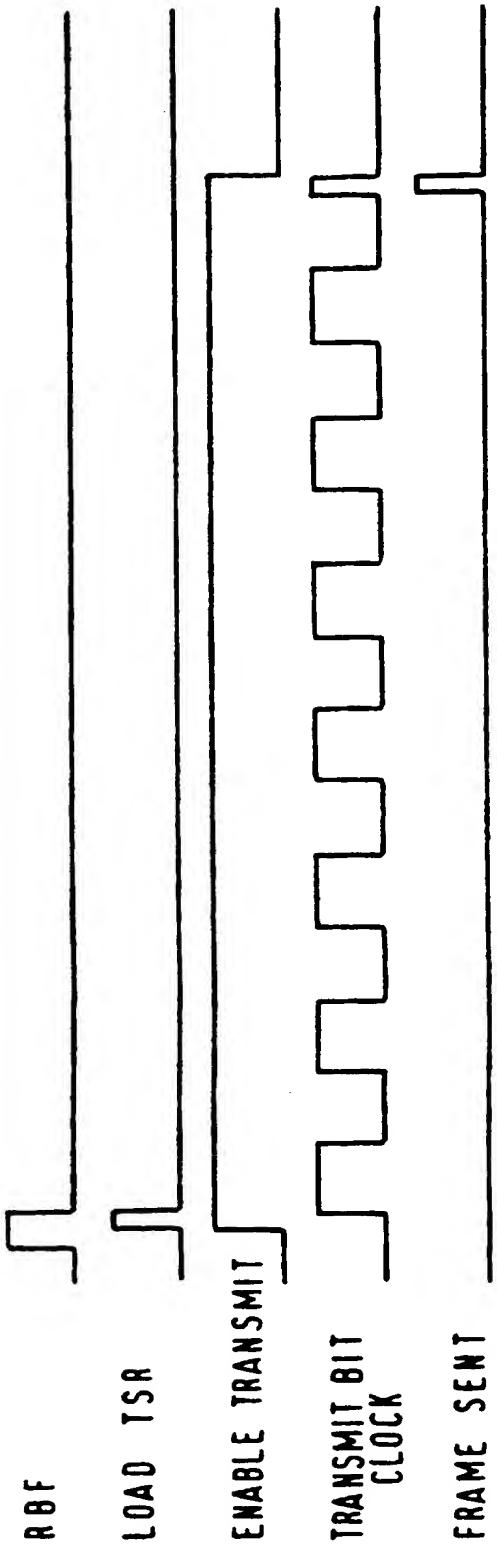

DATA IN
START BIT
ENABLE RECEIVE
RECEIVE BIT CLOCK
RSR FULL
LOAD RB

FIG.10


RBF
LOAD TSR
ENABLE TRANSMIT
TRANSMIT BIT CLOCK
FRAME SENT

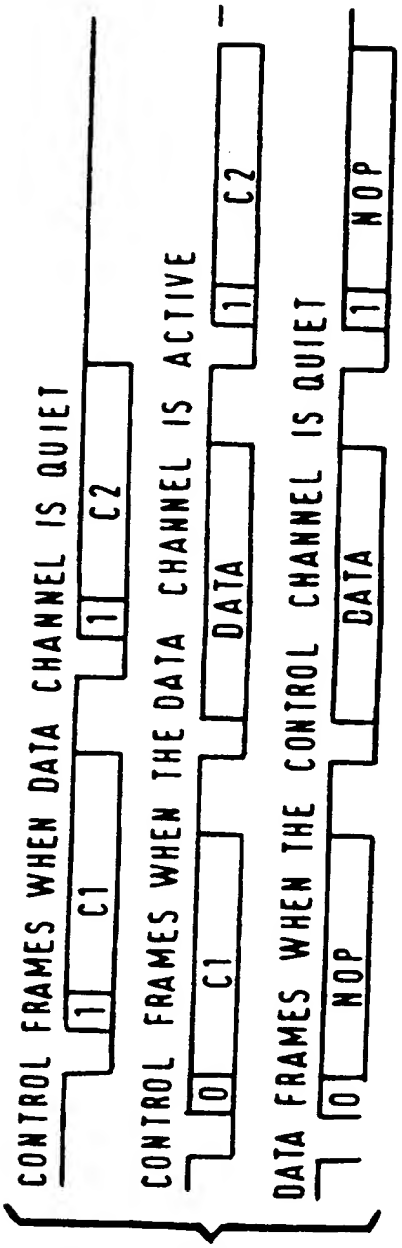


FIG.12

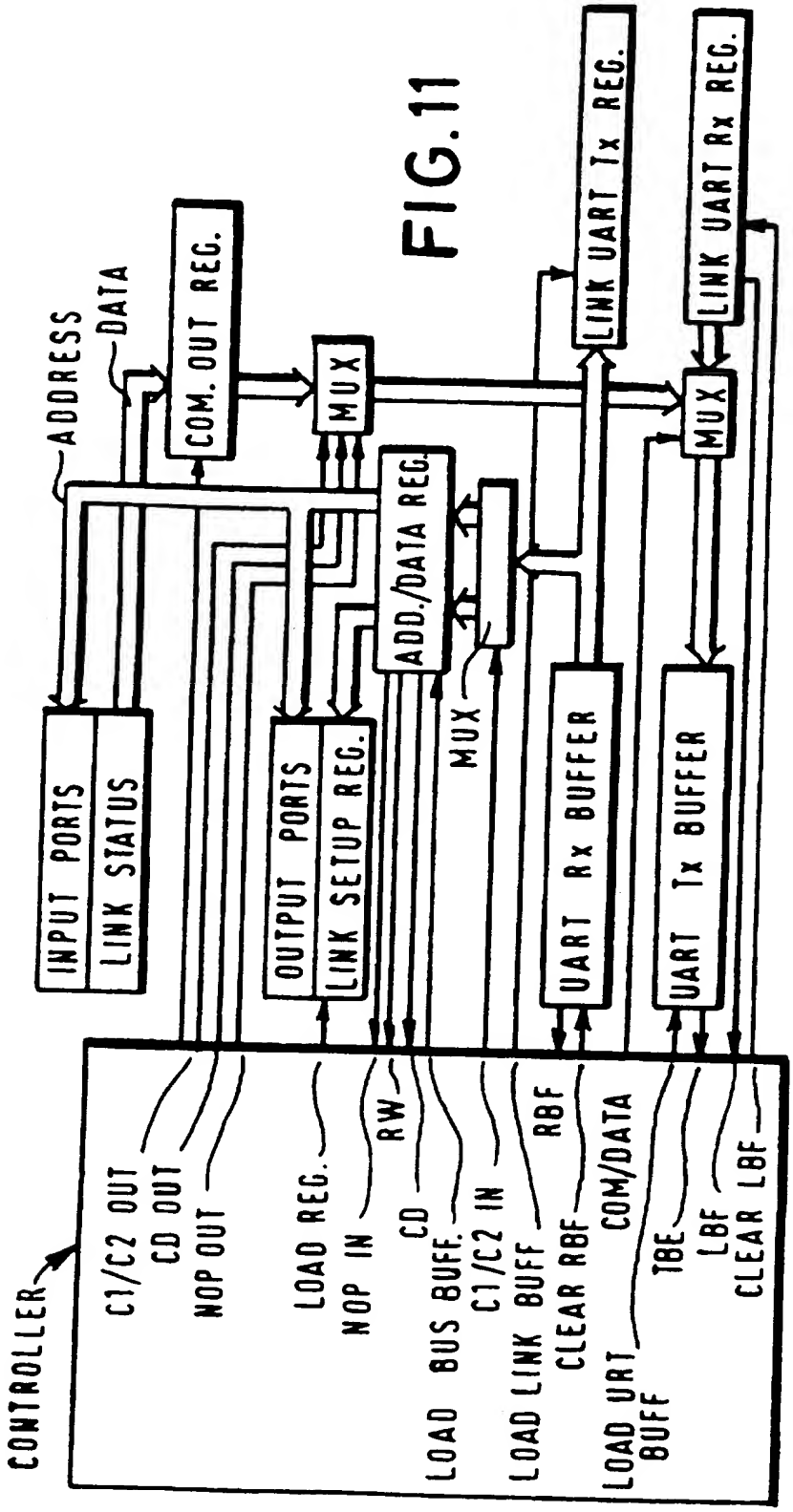


FIG.11

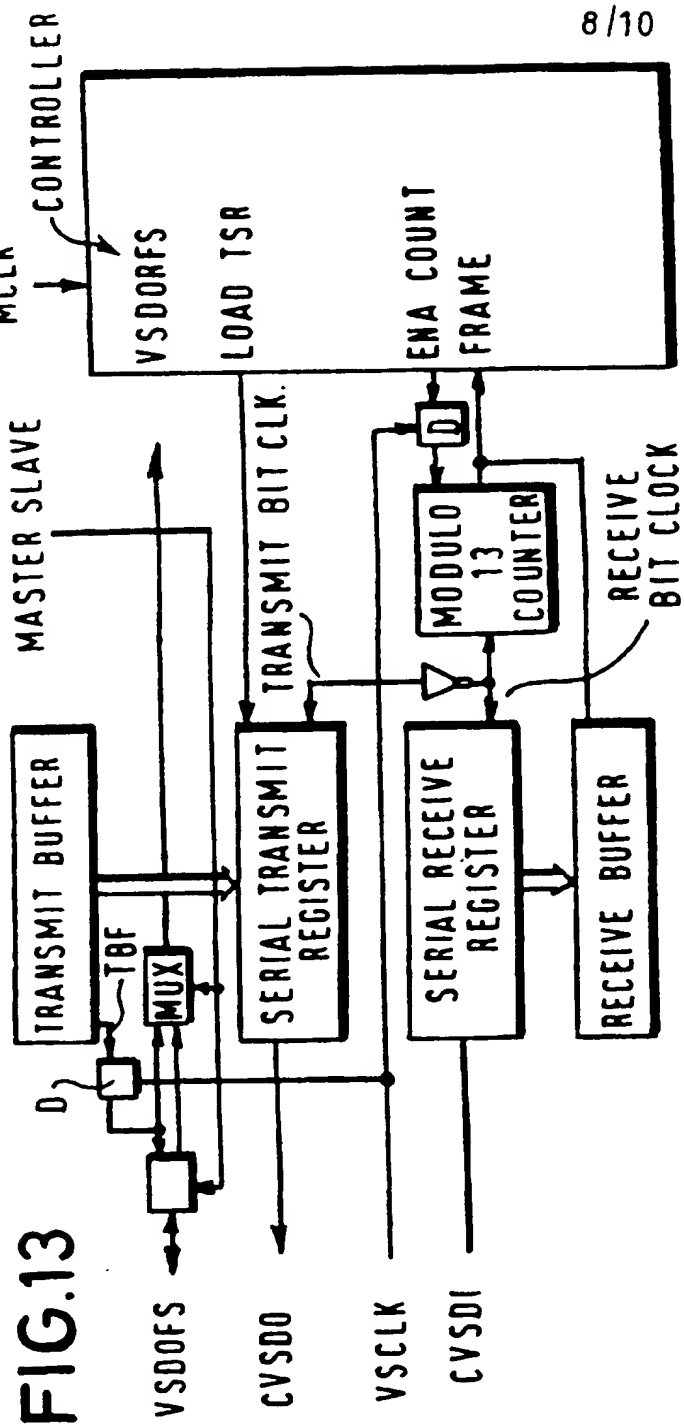

CONTROLLER
MCLK
VSDORFS
LOAD TSR
ENA COUNT
FRAME
MASTER SLAVE
TRANSMIT BIT CLK.
MODULO 13 COUNTER
RECEIVE BIT CLOCK
TRANSMIT BUFFER
TBF
MUX
SERIAL TRANSMIT REGISTER
SERIAL RECEIVE REGISTER
RECEIVE BUFFER
D
VSDOFS
CVSDO
VSCLK
CVSDI

FIG.13

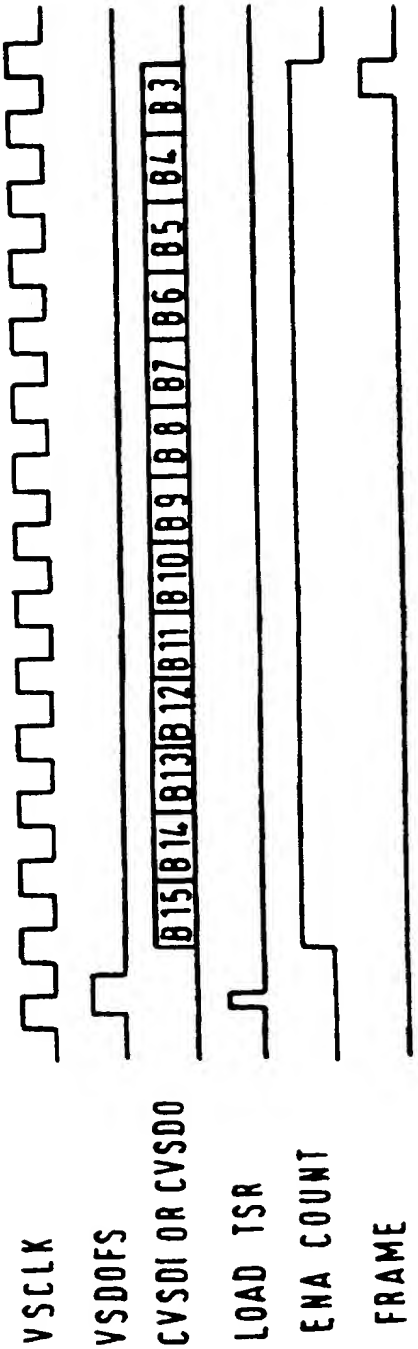

VSCLK
VSDOFS
CVSDI OR CVSDO
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3
LOAD TSR
ENA COUNT
FRAME

FIG.14

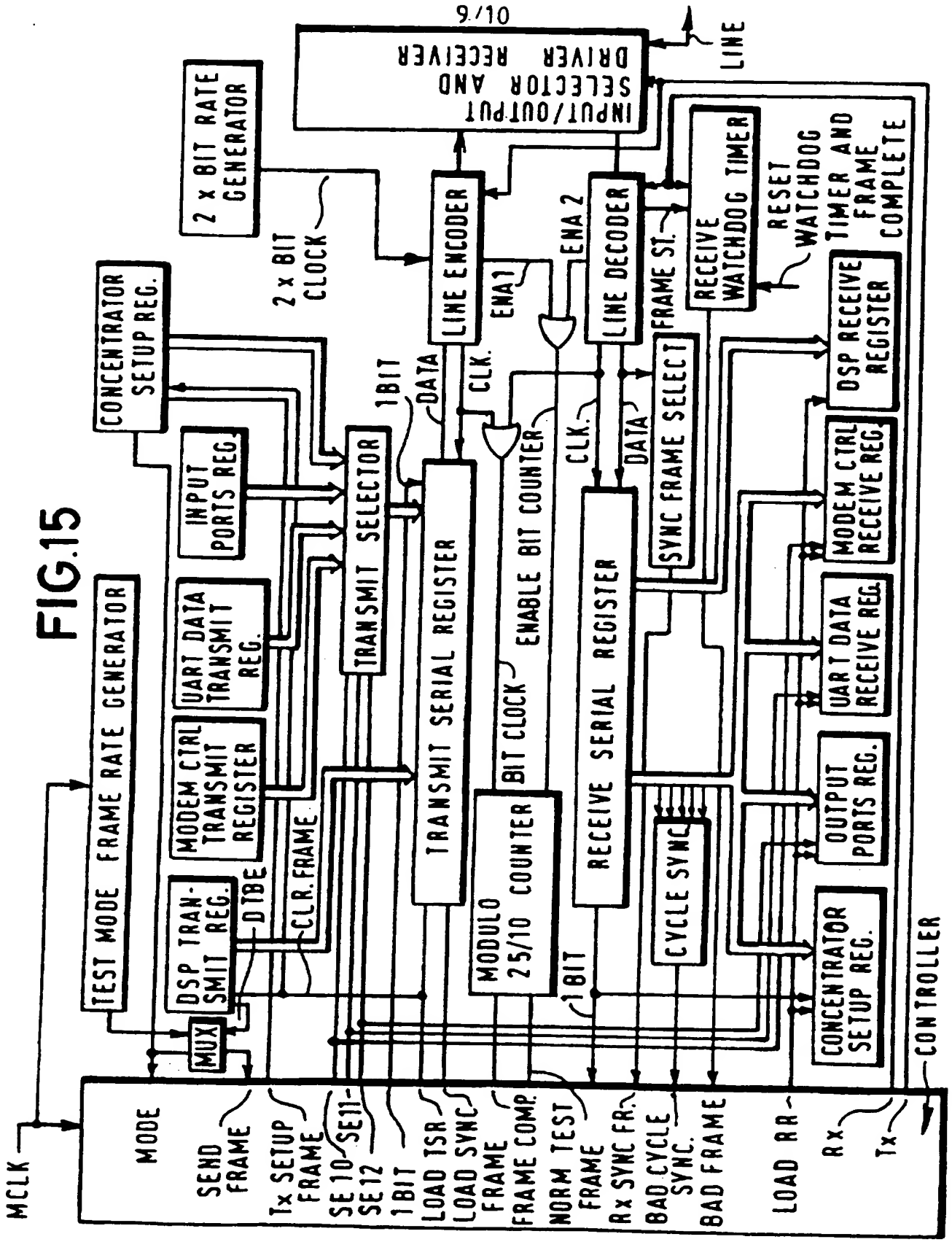

MCLK
MODE
SEND FRAME
Tx SETUP FRAME
SE10
SE11-SE12
1BIT
LOAD TSR
LOAD SYNC FRAME
FRAME COMP.
NORM TEST FRAME
Rx SYNC FR.
BAD CYCLE SYNC.
BAD FRAME
LOAD RR
Rx
Tx
CONTROLLER
TEST MODE FRAME RATE GENERATOR
MUX
DSP TRANSMIT REG.
DTBE
MODEM CTRL TRANSMIT REGISTER
CLR.FRAME
UART DATA TRANSMIT REG.
INPUT PORTS REG.
CONCENTRATOR SETUP REG.
TRANSMIT SELECTOR
1BIT DATA
TRANSMIT SERIAL REGISTER
CLK.
BIT CLOCK
ENABLE BIT COUNTER
MODULO 25/10 COUNTER
1BIT
CLK.
DATA
RECEIVE SERIAL REGISTER
SYNC FRAME SELECT
CYCLE SYNC
FRAME ST.
RECEIVE WATCHDOG TIMER
RESET WATCHDOG TIMER AND FRAME COMPLETE
DSP RECEIVE REGISTER
MODEM CTRL RECEIVE REG.
UART DATA RECEIVE REG.
OUTPUT PORTS REG.
CONCENTRATOR SETUP REG.
2 x BIT CLOCK
2 x BIT RATE GENERATOR
LINE ENCODER
ENA1
ENA 2
LINE DECODER
INPUT/OUTPUT SELECTOR AND DRIVER RECEIVER
LINE

FIG.15

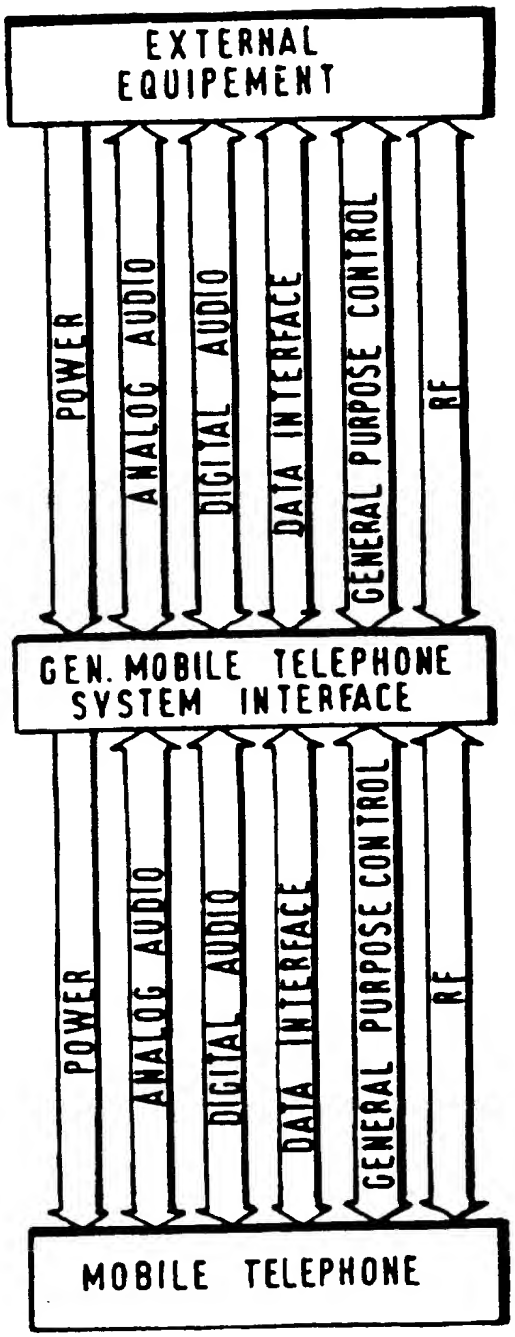

EXTERNAL EQUIPEMENT
POWER
ANALOG AUDIO
DIGITAL AUDIO
DATA INTERFACE
GENERAL PURPOSE CONTROL
RF
GEN. MOBILE TELEPHONE SYSTEM INTERFACE
POWER
ANALOG AUDIO
DIGITAL AUDIO
DATA INTERFACE
GENERAL PURPOSE CONTROL
RF
MOBILE TELEPHONE

FIG.16

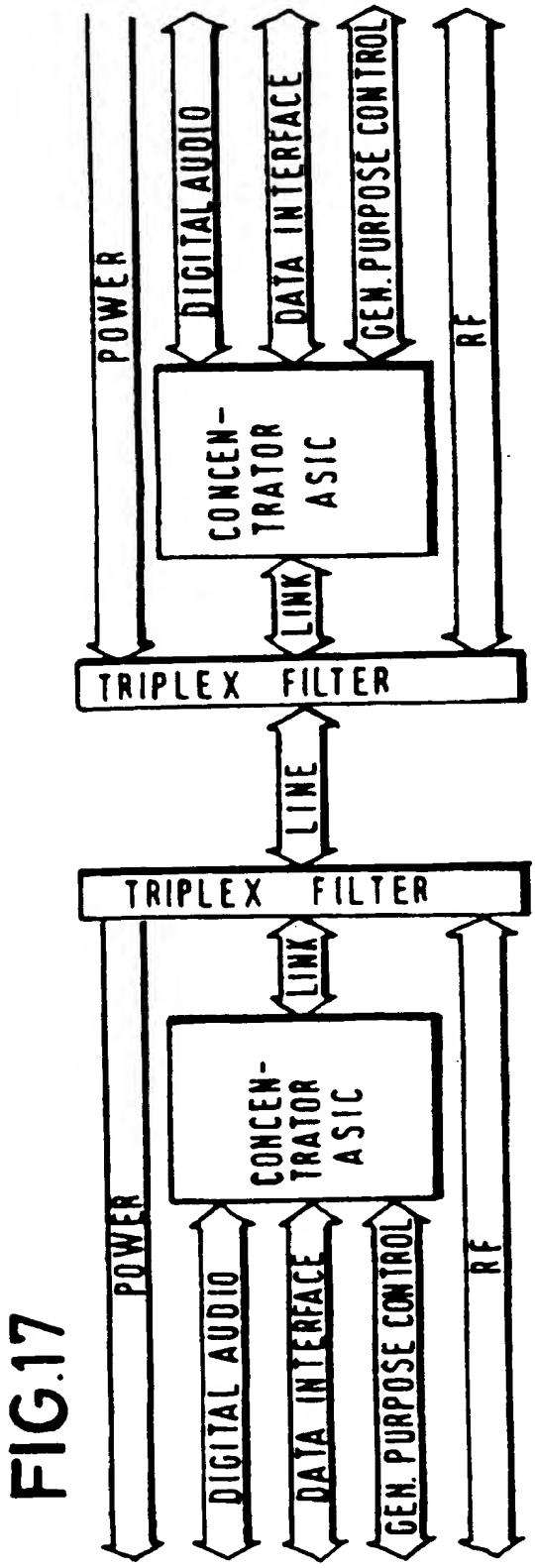

POWER
DIGITAL AUDIO
DATA INTERFACE
GEN. PURPOSE CONTROL
RF
CONCEN-TRATOR ASIC
LINK
TRIPLEX FILTER
LINE
TRIPLEX FILTER
LINK
CONCEN-TRATOR ASIC
POWER
DIGITAL AUDIO
DATA INTERFACE
GEN. PURPOSE CONTROL
RF

FIG.17

INTERNATIONAL SEARCH REPORT

Intern. al Application No
PCT/GB 97/01151

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 237 570 A (SMOLINSKE JEFFREY C ET AL) 17 August 1993	1
A	see column 3, line 53 - column 4, line 55 see column 5, line 54 - column 7, line 9 see column 7, line 58 - line 67 see column 8, line 63 - column 11, line 55; figures 2-4,6	4,7-9,11

A	EP 0 655 873 A (NOKIA MOBILE PHONES LTD) 31 May 1995 see page 2, line 38 - line 48 see page 2, line 53 - page 3, line 6	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 August 1997	03.09.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Bossen, M

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. al Application No
PCT/GB 97/01151

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		BR 9205348 A	31-05-94
		CA 2087839 A	19-01-93
		CN 1068923 A	10-02-93
		DE 4292401 C	02-02-95
		FR 2681743 A	26-03-93
		GB 2263847 A,B	04-08-93
		IT 1258436 B	26-02-96
		JP 2562791 B	11-12-96
		JP 6502056 T	03-03-94
		SE 9300877 A	18-05-93
		WO 9302531 A	04-02-93
EP 0655873 A	31-05-95	FI 935347 A	31-05-95
		DE 655873 T	15-05-97
		ES 2096537 T	16-03-97